Approval: 1st Convocation Adhoc Meeting

Course Title: Analog Electronics Lab
Course No.: EE 202P
Credits : 0-0-2-1
Prerequisites:
Students intended for : B.Tech.
Elective or Compulsory
Semester : Odd/Even
Course Contents:

Lab 1: Introduction to Spice and Winspice

Lab 2: Construct a spice netlist to study the characteristics of a BJT. Do a dc analysis and sweep the base current and illustrate the dependence of beta on collector current.

Lab3: Construct spice netlist to analyse the sensitivity of Quiscent current for

a) Simple resistor biasing, b) Voltage divider biasing, c) Emitter degeneration biasing

d) Self biasing

Prepare a report and discuss the biasing schemes based on your sensitivity analysis results.

Lab 4:

The common-emitter shown in the figure must amplify signals in the range of 1 MHz to 100 Mhz.

(a) Using the .op command, determine the bias conditions of Q1 and verify that it operates in the active region.

(b) Running an ac analysis, choose the value of C_1 such that $|V_p/V_{in}| \sim 0.99$ at 1 MHz. This ensures that C1 acts as a short circuit at all frequencies of interest.

(c) Plot |Vout/Vin| as a function of frequency for several values of C2 , e.g., 1 uF, 1 nF, and 1 pF. Determine the value of C2 such that the gain of the circuit at 10 MHz is only 2% below its maximum (i.e., for C2 = 1uF).

(d) With the proper value of C2 found in (c), determine the input impedance of the circuit at 10 MHz. (One approach is to insert a resistor in series with Vin and adjust its value until VP/Vin or Vout/Vin drops by a factor of two.)