Approval: OTA in 2nd Convocation Meeting

Course No.: EE-678

Course Name: Digital Circuit Design

Credits: 3

Course Outline:

Review: Basic MOS structure and its static behaviour; Quality metrics of a digital design: Cost, functionality, robustness, power, and delay. CMOS Inverter: Static CMOS inverter, switching threshold and noise margin concepts and their evaluation, dynamic behaviour, power consumption and effect of scaling on CMOS performance metrics. CMOS Combinational Logic: Static CMOS design, ratioed logic, pass transistor logic, dynamic logic, speed and power dissipation in dynamic logic, cascading dynamic gates, CMOS transmission gate logic. CMOS Sequential Logic: Static latches and registers, bistability principle, MUX based latches, static SR flip-flops, master-slave edge-triggered register, dynamic latches and registers, concept of pipelining, pulse registers, nonbistable sequential circuit. Timing Issues: Synchronous timing basics, classification, skew and jitter, and their sources, clock distribution techniques, self-timed circuit design, synchronisers and arbiters, clock synthesis and synchronization using PLL. Design of Arithmetic Building Blocks: Adder, multiplier, shifter, and other operators; Power and speed trade-off in datapath structures. 5 0 3 0 0 15 00 35 50 00 0 3 √7. Memory and Array Structure: Core, ROM, RAM, peripheral circuitry, memory reliability and yield, SRAM and DRAM design, evaluation of RNM and WNM from butterfly curves, flash memory.